Claims

1. A drive circuit to supply drive current to a load resistor that is connected to a first power voltage supply element, comprising:

a current output MOS transistor connected in series with the load resistor,

a drive part that is connected to a second power voltage supply element and that supplies a drive signal to the gate terminal of the current output MOS transistor, and

a clamp circuit that is connected to the second power voltage supply terminal to hold the drain terminal of the current output MOS transistor at a predetermined potential.

2. The drive circuit of Claim 1 wherein the clamp circuit comprises:

a first MOS transistor that is connected between the gate terminal and the drain terminal of the current output MOS transistor,

a second MOS transistor in which the gate terminal and the drain terminal are connected together and in which said gate terminal is connected to the gate terminal of the first MOS transistor,

a rectifying element that is connected between the gate terminal of the current output MOS transistor and the first MOS transistor, or between the first MOS transistor and the drain terminal of the current output MOS transistor, and

a voltage holding circuit that is connected to the source terminal of the second MOS transistor and that holds the potential of said source terminal at a predetermined voltage.

3. The drive circuit of Claim 2, wherein the clamp circuit has a first current source that supplies current to the second MOS transistor,

the current output MOS transistor and the first and second MOS transistors are NMOS transistors, and

the voltage holding circuit is a plurality of diodes connected in series between the source terminal and the reference potential of the second NMOS transistor.

4. The drive circuit of Claim 3, wherein the first current source has a first PMOS transistor that is connected between the second power supply voltage terminal and the drain terminal of the second NMOS transistor, a second PMOS transistor where the gate terminal and drain terminal are connected to each other, where said gate terminal is connected to the gate terminal of the first PMOS transistor, and where the source terminal is connected to the second power supply voltage terminal, and a first resistive element that is connected between the drain terminal and the reference potential of the second PMOS transistor.

5. The drive circuit of Claim 3, wherein the rectifying element is a diode whose anode is connected to the gate terminal of the current output NMOS transistor and whose cathode is connected to the drain terminal of the first NMOS transistor.

6. The drive circuit of Claim 3, wherein the rectifying element is a third NMOS transistor that is connected between the drain terminal of the current output NMOS transistor and the source terminal of the first NMOS transistor, and whose gate terminal is connected to the drain terminal of the first NMOS transistor.

7. The drive circuit of Claim 1, wherein the drive part includes:

a fourth MOS transistor that is connected to the gate terminal of the current output MOS transistor and that supplies a drive signal to the current supply MOS transistor, and

a second current source that supplies current to the fourth MOS transistor.

8. The drive circuit of Claim 7 wherein the drive part comprises a third current source that is connected between the source terminal and the reference potential of the fourth MOS transistor, which is an NMOS transistor, and a fifth NMOS transistor that is connected between the second current source and the reference potential and that operates complementarily with the fourth NMOS transistor, and

the second current source comprises a third PMOS transistor that is connected between the second power supply voltage terminal and the fifth NMOS transistor and

whose gate terminal and drain terminal are connected, and a fourth PMOS transistor that is connected between the second power supply voltage terminal and the middle connection point between the gate terminal of the current output MOS transistor and the fourth NMOS transistor, and whose gate terminal is connected to the gate terminal of the third PMOS transistor.

9. The drive circuit of Claim 8 wherein the drive part has a second resistive element that is connected between the drain terminal of the third PMOS transistor and the drain terminal of the fifth NMOS transistor, and a third resistance terminal that is connected between the second power supply voltage terminal and the gate terminal of the third PMOS transistor.